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1. Your reference

4/P32252GB

2. Patent application number
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13 NOV 1998 **9824989.9**

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

University of Surrey
Guildford
Surrey
GU2 5XH

Patents ADP number *(if you know it)*

79851200 1

If the applicant is a corporate body, give the country/state of its incorporation

U.K.

4. Title of the invention

ANTI-JITTER CIRCUITS

5. Name of your agent *(if you have one)*

MATHISEN, MACARA & CO.

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

The Coach House
6-8 Swakeleys Road
Ickenham,
Uxbridge UB10 8BZ

Patents ADP number *(if you know it)*

1073001

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Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*
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Number of earlier application	Date of filing *(day / month / year)*

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PATENT APPLICATION

COUNTRY: G.B.

APPLICANTS: UNIVERSITY OF SURREY

FORMAL TITLE: ANTI-JITTER CIRCUITS

SHORT TITLE: ADIABATIC AJC
MM REFERENCE NO: P32252GB

APPLICATION NO

FILED:

PRIORITY CLAIMED:

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<u>Agents for the Applicants</u>

ANTI-JITTER CIRCUITS

This invention relates to anti-jitter circuits (AJC).

An AJC is described in our European patent application No. 97903456.8 based on International patent application, publication No. WO 97/30516. The described AJC circuit provides a unique way of reducing phase noise or time jitter on a frequency source, typically 20 dB or more for the or each (fully cascaded) stage. Figures 1(a) to 1(c) of the accompanying drawings illustrate the principle of operation of this earlier AJC. Figure 1(a) is a block circuit diagram of the system described in the earlier patent application, Figure 1(b) shows an input pulse train with jitter (shown in broken outline) on the central pulse and Figure 1(c) shows the corresponding integrator output (Op2) and the comparator switching level (Op1).

The present invention provides an improvement over this earlier AJC. Because the implementation of the core part of the improved AJC requires no d.c. power the term adiabatic anti-jitter circuit (AAJC) will be used hereinafter.

According to the invention there is provided an anti-jitter circuit for reducing time jitter in an input pulse train comprising:

an integrator charge storage means,

charging means for deriving from the input pulse train at least one charge packet

during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means, and

discharging means for continuously discharging the integrator charge storage means,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage waveform having a mean d.c. voltage level, and

means for comparing said time varying voltage waveform with said mean d.c. voltage level and deriving an output pulse train as a result of the comparison.

Anti-jitter circuits according to the invention are now described, by way of example only, with reference to the accompanying drawings in which:

Figures 1(a) to 1(c) illustrate a known anti-jitter circuit described in our International patent application, publication number WO 97/30516,

Figures 2(a) to 2(d) illustrate an embodiment of an anti-jitter circuit according to the present invention,

Figures 3(a), 3(b); 4(a), 4(b) and 5(a), 5(b) illustrate further embodiments of the anti-jitter circuit shown in Figures 2(a) to 2(d),

Figure 6 shows an anti-jitter circuit according to the invention in which the pulse length of an output monostable circuit is controlled,

Figure 7 shows an anti-jitter circuit according to the invention having a frequency doubling input, and

Figures 8 and 9 show anti-jitter circuits according to the invention including circuitry arranged to maintain the charge value of charge packets substantially constant.

The principle of operation can be seen by reference to Fig 2 and it has some similarities to that of a charge pump. An approximately constant charge packet is formed either once or, in a second variation of the scheme, twice per input frequency source cycle. Each charge packet adds to the charge in an integrator storage capacitor C3. A controlled current source T1 (or more accurately current sink) discharges the capacitor C3 at a rate that maintains a substantially constant mean dc voltage level on the integrator storage capacitor C3. A high impedance low pass filter (R1, C4) connected to the integrator storage capacitor C3 establishes the mean dc voltage level that then controls the discharge current in a negative feedback configuration. The combination of intermittent charging and continuous discharging creates a sawtooth voltage waveform Op2 on the integrator storage capacitor C3. The two (high impedance) inputs of a differential comparator (not shown) are connected respectively to the input and output of the low pass filter. This establishes switching points when the mean dc level Op3 is equal to the sawtooth voltage waveform present on the integrator storage capacitor C3. The switching point on the discharge part of the sawtooth waveform has very much reduced timing jitter (as described in the aforementioned publication). This discharge switching transition then triggers an output monostable or divide-by-two circuit, as described in that publication.

The combination of the negative feedback and the differential comparator means that the correct comparator switching levels are established automatically for a very wide range

of input frequencies without any change of circuit components values.

When the diodes D5 to D8 in Fig 2 are not conducting, the time constant R1C3C4/(C3+C4) determines the sideband frequency below which the jitter suppression starts to degrade at a 6dB per octave rate. The optimum loop gain is found to be gmR1 $= (C3+C4)^2/C3C4$. For a FET we have gm $= \sqrt{(2I_{dis}\beta)}$ and from the explanation below it can be seen that $I_{dis}=f_{ina}Q$, that is proportional to input frequency. The consequence is that the loop gain varies as the square root of input frequency. For such a control loop the loop gain can typically be allowed to vary by up to four to one with little variation in overall settling time or loop bandwidth. This then corresponds to a working frequency range of sixteen to one with no changes in component values.

Four optional "speed up" diodes D5 to D8 shown across the resistor R1 provide a low impedance path from input to the output shunt capacitor C4 of the low pass filter if the positive or negative voltage exceeds 2 diode (Vbe) offset levels (approximately 2 x 0.6 volts typically). This option lowers the time constant of the low pass filter by orders of magnitude during initial acquisition of lock of output signal to input signal, or if large frequency or phase jump deviations occur in the input signal. The time for initial acquisition is thus much reduced and input to output lock is maintained (with no input pulses missed) over a wider range of input deviations of phase or frequency. The presence of the diodes also allows phase jitter sideband components much closer to carrier to be better suppressed after a full settling has occurred.

In the case of the charge pump arrangement of diodes D1 and D2, and input capacitor C1 in Fig 2(a), the peak-to-peak amplitude V_{ppst} of the sawtooth waveform is given approximately by the relationship $Q = C_3 V_{ppst} = C_1 V_{ppin}$, where V_{ppin} is the peak-to-peak input voltage and C_3 is the integrator storage capacitance. Q is actually the quantity of charge being transferred from C1 to C3 each time a transfer occurs. A large phase jitter adds substantially to the peak-to-peak voltage swing whilst two diode offsets should be subtracted from V_{ppin} to obtain a more accurate relationship. This relationship is used to ensure that the worst case V_{ppst} for the sawtooth is sufficiently less than 4 (Vbe) diode offsets range between the switch on levels of the speed up diodes D5 to D8.

Conveniently controlled current source T1 is a transistor in the form of an insulated gate FET (as shown in Fig 2(a)). Alternatively a high input impedance bipolar transistor combination such as a Darlington arrangement may be used in place of T1. A high input impedance is desirable so that a long time constant (or low cut off frequency) can be obtained for the low pass filter and at the same time keeping the value of the filter capacitor C4 to a low value. For fastest speed up acquisition time, C4 is made comparable in value to charge pump and storage capacitors C1 and C3.

The mean diode discharge current I_{dis} is given by the relationship $I_{dis} = f_{ina} Q$ where the charge packet Q has been defined in the above and f_{ina} is the rate of input frequency active transitions. Thus the FET or transistor characteristics should be chosen to provide this current at the desired mean sawtooth voltage. The value of the resistor R2 can also be

conveniently chosen to reach this desired design objective; particularly there is a constraint on the choice of transistor characteristics. For a given transistor choice the resistor R2 can also be conveniently chosen to give a typical 10 to 1 operating frequency range anywhere within a design envelope of typically 1000 to 1, without having to alter the value of any other component within the circuit.

Figs 3 and 4 demonstrate by simulation the extreme frequency range limits of the AAJC shown in Figure 2 when only the resistor R2 is varied. However, purely for the purpose of display of aquisition within a limited number of input waveform cycles, the time constant C4R1 has been appropriately chosen in each case. Fig 5 shows the AAJC simulation operating of 5GHz. In all cases the waveforms are for operation starting from initial switch on. The acquisition time is when the two waveforms of Op2 and Op3 intersect with no further missed intersections.

As an additional improvement, shown in Figure 6, the mean d.c. output from the low pass filter (being a direct function of may be frequency) can be used directly or through a matched current mirror process to control the pulse length of an output monostable. In this way the overall circuit can be made self-adjusting in terms of maintaining a good output waveform mark space ratio over a wide frequency range. A circuit arrangement for this is regarded as existing state of the art.

All the power for the AAJC circuit is obtained from the input source. An approximate

estimate for the power dissipated in the circuit is the product of the discharge current and the mean d.c. voltage. Given ideal components there are no other dissipative processes in the circuit. A safer limit allowing for other losses would be to take the product of the input voltage swing and the discharge current.

A typical AAJC would operate with a discharge current of less than 1 to 2mA with a 5 volt input swing. In this example the input source would have to provide a maximum of 10mW.

In addition it is advantageous if the source waveform rise and fall times are short. Times of less than about one tenth of an average period minimise potential amplitude to phase conversion of any noise appearing at the input.

The amplitude of the input waveform should be reasonably constant over the short term. However it is a feature of the circuit that it automatically adjusts for long term (low frequency) variations in the input amplitude.

A frequency doubling circuit can be implemented in a very simple way with the AAJC as shown in Fig 7, 8 and 9. Here there are two input charge pumps C1, D1; C2, D2 which operate alternately on the rising and falling edges of the input waveform. The transformer XMR, is shown by way of example only and may be replaced by some transformerless push pull active circuit operating on the input signal. Advantages of frequency doubling

and then dividing to obtain the final output are a further 6dB of phase noise reduction and an equal output mark space ratio which is retained over the whole frequency range of operation.

A disadvantage of the simple diode charge pump as shown is that the value of the charge packets is approximately proportional to the voltage existing on the integrator storage capacitor at the start time of the charge packets. Thus to obtain the best jitter reduction it is advisable to keep the peak-to-peak sawtooth voltage as a small percentage as possible of the mean voltage. Figs 8 and 9 show a frequency doubling circuit where the charge packets are kept much more constant by the presence of transistor T2 and its base components C5 and R3 which perform an averaging function over a few input cycles. The transistor operates essentially in the grounded base mode while conveying charge. Since the base voltage stays constant over several input cycles any phase jumps causing the mean level of the sawtooth waveform to vary do not cause the size of the charge packets to vary. The input capacitors C1 and C2 are charged or discharged into constant voltage sinks. Obviously this technique also applies to the basic circuits as well where frequency doubling is not implemented.

Fig 9 shows a more convenient arrangement if T2 is a FET. The time constant components C5 and R3 are no longer required because the gate of T2 is connected to the gate of T1.

Transistors T2 in Fig 8 and Fig 9 are the most likely devices to restrict the upper frequency operation of the circuit. Because the mobility of holes is less than for electrons it may be advantageous to exchange p-devices for n-devices (or pnp for npn) and vice versa and at the same time reverse the sense of the input diodes. It is likely in practice that this will result in somewhat higher maximum frequency of operation.

Particularly advantageous aspects of the described embodiments include:

1. An input source having approximately constant amplitude. It is also desirable, but not essential, that the input waveform should have a risetime no longer than about one tenth of an average period of the input waveform. Circuit performance in practice is then found to be improved.

2. An input capacitor C1 (or pair of input capacitors C1 and C2) to form an input charge packet of substantially constant charge value when switched at one terminal by the aforesaid input signal.

3. An integrator capacitor that is charged by constant charge packets at the input frequency rate, and

4. permanently discharged by a controlled discharge current source or sink. The discharge device can be almost any transistor having a reasonably high output impedance

for its drain or collector.

5. A low pass filter (typically a single section RC filter) connected to form a negative feedback path from the storage capacitor to the control input (gate or base) of the controlled current source.

6. The negative feedback connection causes a substantially constant mean d.c. level to exist on the storage capacitor. The feedback thus performs the function of d.c. removal so that the storage capacitor, considered as an integrator of the charge and discharge currents, is not affected by d.c. drift.

7. A differential comparator with one input connected to, and responsive to the sawtooth waveform on, the storage capacitor. And the other input connected to the mean d.c. level (at the output of the low pass filter).

8. A triggered output circuit as described in the aforementioned publication, connected to be triggered only by the low jitter output transition of the comparator. (The low jitter transition occurs on the slower of the two sawtooth waveform slopes).

9. Back to back speedup diodes (D5 to D8) can be connected to form a low impedance path between the input and output of the feedback low pass filter for the case when input phase jumps cause the integrator voltage to jump out of limits set by the

number of diodes in series and the typical diodes offset voltages.

10. A frequency doubling input circuit in which two charge pumps operate alternately on the rising and falling edges of the input waveform and convey their charge packets via a common path to the storage capacitor.

11. (a). A common gate or common base transistor circuit connected in the path between the input capacitor(s) and the storage capacitor, so that better constancy of charge packets in ensured.

(b). A time constant also connected to the base that ensures constancy of charge packet size in the short term fluctuations in input signal amplitude. Or the gate of T2 connected to the gate of T1.

12. The use of the low pass filter output voltage (which is known function of frequency) to keep the mark space ratio of an output monostable essentially constant for a wide range of input frequencies. A FET can alternatively be connected to the gate of T1 mirror the current of T1 to a current controlled output monostable to achieve the same objective.

CLAIMS

1. An anti-jitter circuit for reducing time jitter in an input pulse train comprising,

an integrator charge storage means,

charging means for deriving from the input pulse train at least one charge packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means, and

discharging means for continuously discharging the integrator charge storage means,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage waveform having a mean d.c. voltage level, and

means for comparing said time varying voltage waveform with said mean d.c. voltage level and deriving an output pulse train as a result of the comparison.

2. An anti-jitter circuit as claimed in claim 1 wherein said discharging means comprises a discharge device having a control input and means defining a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage level substantially constant.

3. An anti-jitter circuit as claimed in claim 2 wherein said discharge device is a current source or a current sink.

4. An anti-jitter circuit as claimed in claim 3 wherein said discharge device is a transistor.

5. An anti-jitter circuit is claimed in any one of the claims 2 to 4 wherein said means defining a negative feedback path comprises a low pass filter.

6. An anti-jitter circuit as claimed in claim 5 wherein the negative feedback path is formed by the combination of a resistor and a capacitor.

7. An anti-jitter circuit as claimed in claim 5 or claim 6 wherein said mean d.c. voltage level is generated at an output of said negative feedback path and said means for comparing comprises a comparator having a first input coupled to the integrator charge storage means and a second input coupled to said output of the negative feedback path.

8. An anti-jitter circuit is claimed in any one of the claims 2 to 7 including a monostable circuit connected to the output of said means for comparing.

9. An anti-jitter circuit as claimed in claim 8 wherein said mean d.c. voltage level is used to control the pulse length of pulses output by the monostable circuit.

10. An anti-jitter circuit as claimed in claim 9 wherein the monostable circuit is a current-controlled monostable circuit and has a control input coupled to the output of said

negative feedback path by a current mirror matched to said discharge device.

11. An anti-jitter circuit as claimed in claim 10 wherein said discharge device and said current mirror are matched transistors.

12. An anti-jitter circuit as claimed in any one of claims 8 to 11 wherein said monostable circuit is triggered whenever a discharge part of the time-varying voltage waveform crosses the mean d.c. level.

13. An anti-jitter circuit as claimed in any one of claims 1 to 12 including frequency doubling means comprising a first said charging means and a second said charging means for deriving charge packets respectively from the rising and falling edges of the input pulse train.

14. An anti-jitter circuit as claimed in any one of claims 1 to 13 including means for maintaining the charge value of the charge packets substantially constant.

15. An anti-jitter circuit as claimed in claim 14 wherein said means for maintaining comprises a further transistor coupled between said charging means and said integrator charge storage means.

16. An anti-jitter circuit as claimed in claim 15 wherein said further transistor is

arranged to operate in grounded base mode.

17. An anti-jitter circuit as claimed in claim 16 including averaging means connected to the base of the further transistor.

18. An anti-jitter circuit as claimed in claim 15 wherein said discharging means includes a first field effect transistor operative as a discharge device and said further transistor is a second field effective transistor, and the gate of the first field effect transistor is connected to the gate of the second field effect transistor.

19. An anti-jitter circuit as claimed in any one of claims 2 to 18 including means providing a low impedance path between the input and the output of the negative feedback path.

20. An anti-jitter circuit as claimed in claim 19 wherein said low impedance path is formed by diodes connected back-to-back.

21. An anti-jitter circuit as claimed in any one of the claims 1 to 20 wherein the or each said charging means is a charge pump.

22. An anti-jitter circuit substantially as herein described with reference to Figures 2 to 9 of the accompanying drawings.

ABSTRACT

ANTI-JITTER CIRCUITS (Figure 2)

An anti-jitter circuit has an integrator storage capacitor (C3). A charge pump (C1, D1, D2) derives from an input pulse train at least one charge packet during each cycle of the input pulse train and supplies the charge packets to the storage capacitor (C3). A controlled current sink (T1) operating in conjunction with a high impedance low pass filter (R1, C4) continuously discharges the storage capacitor (C3) to create a sawtooth voltage waveform (Op2) having a mean d.c. voltage level (Op3). A differential comparator compares the sawtooth voltage waveform (Op2) with the mean d.c. voltage level (Op3) and the comparator output is used to trigger a monostable circuit to generate an output pulse train having reduced time jitter.

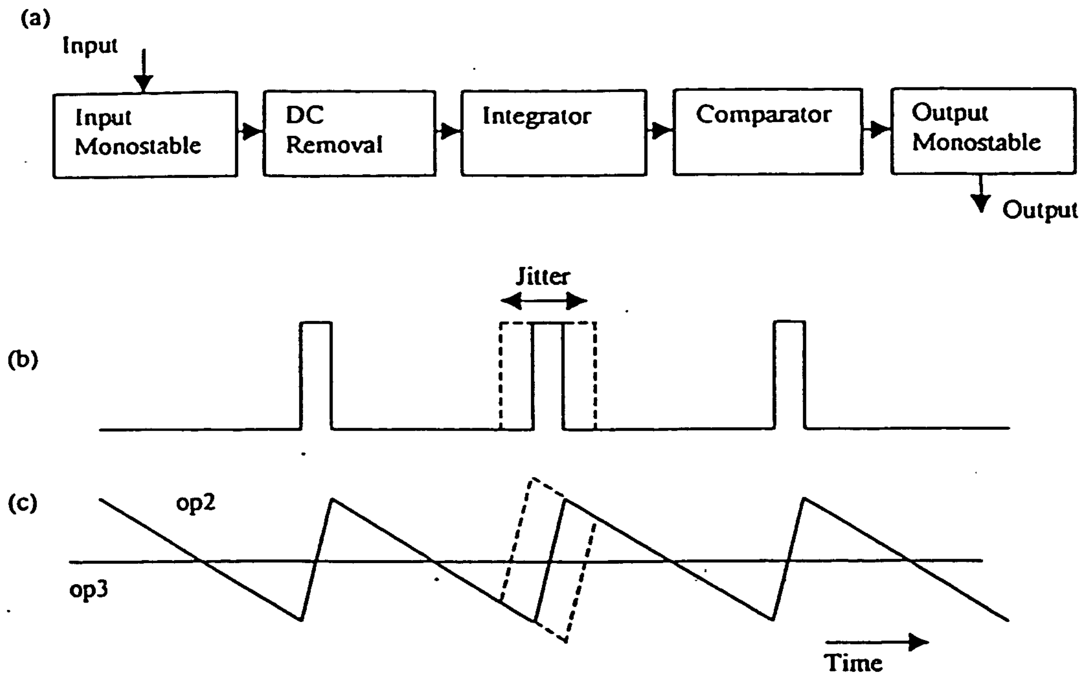
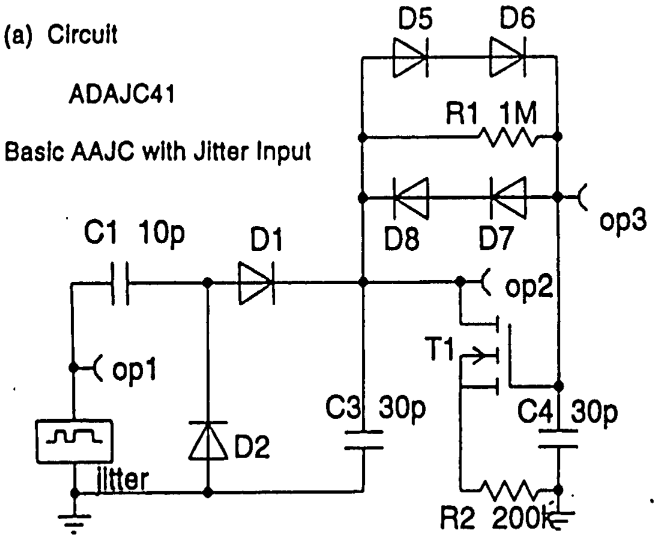


Figure 1. Anti Jitter Circuit Principle: -
(a) Basic Block Diagram
(b) Input with jitter on central pulse
(c) Integrator output (op2) and Comparator switching level (op3)

(a) Circuit

ADAJC41

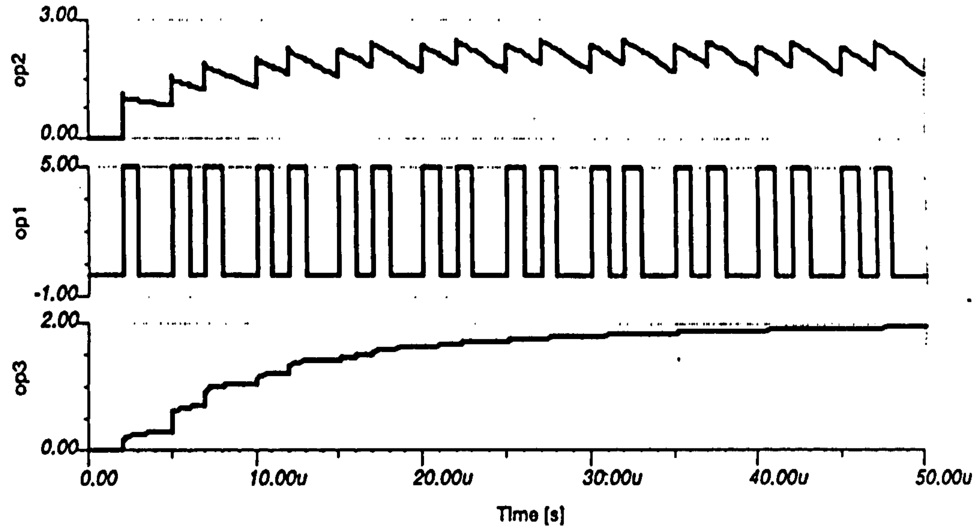
Basic AAJC with Jitter Input



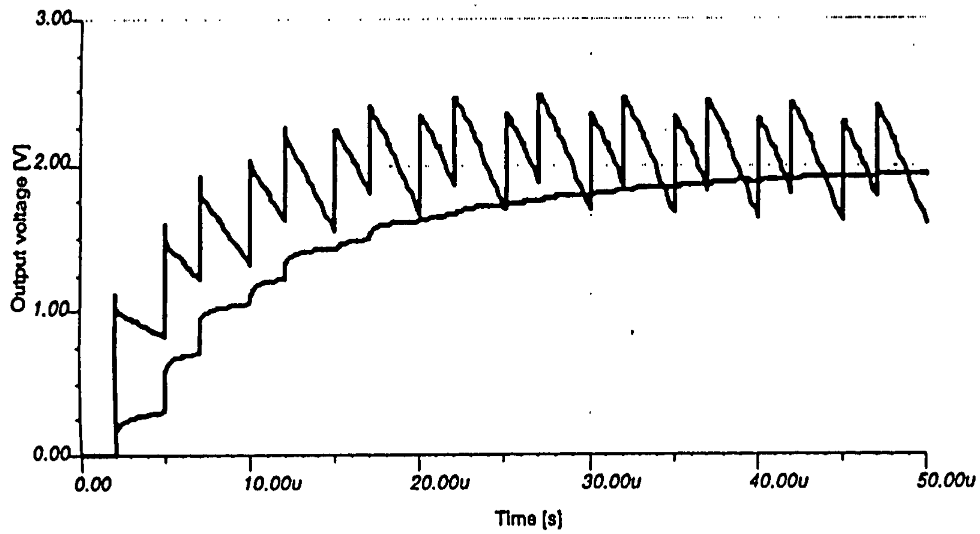
T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

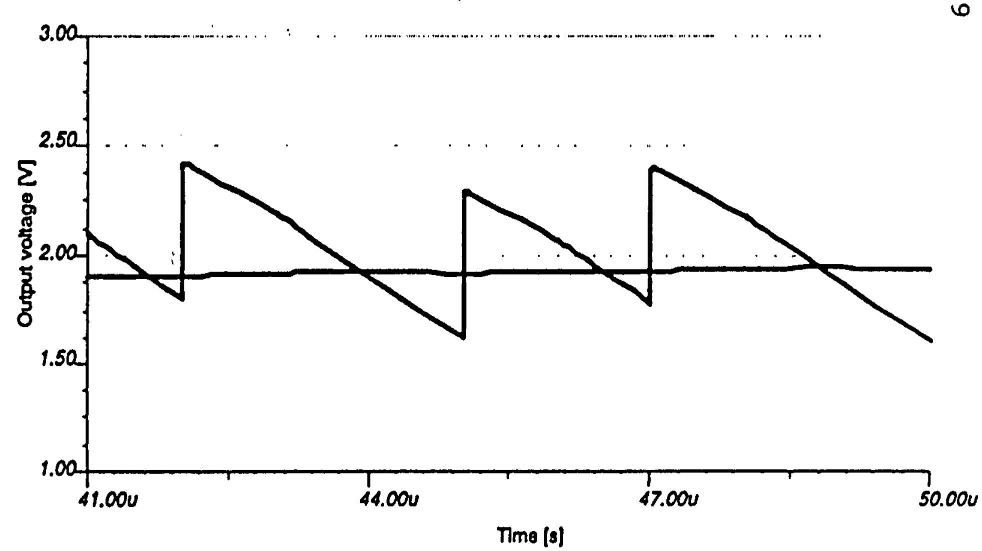
Mean Fin = 417kHz and 1/3 rate phase jumps of ~~300~~ 150 degrees
=Time Jitter of 1usec in 2.4usec at 1/3 rate



(b) op2 = Sawtooth on Integrator Capacitor
op1 = Input
op3 = Mean DC level



(c) op2 and op3 superimposed



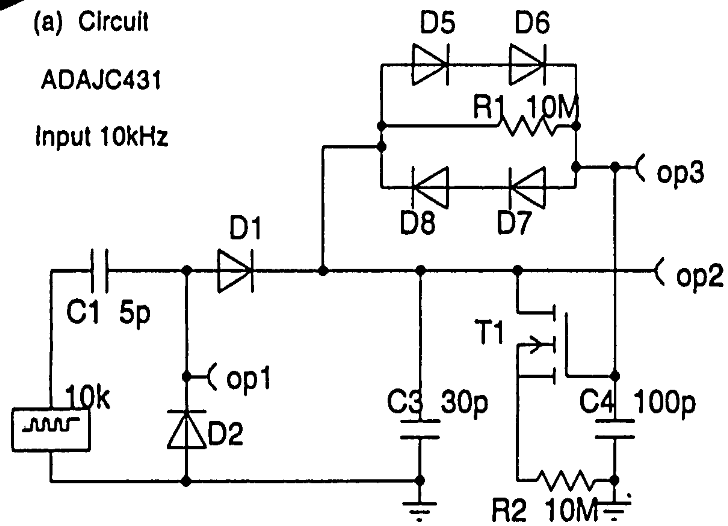
(d) op2 and op3 detail

Fig 2:- (a) Basic Adiabatic AJC (AAJC) and Simulation Results (b) to (d)

(a) Circuit

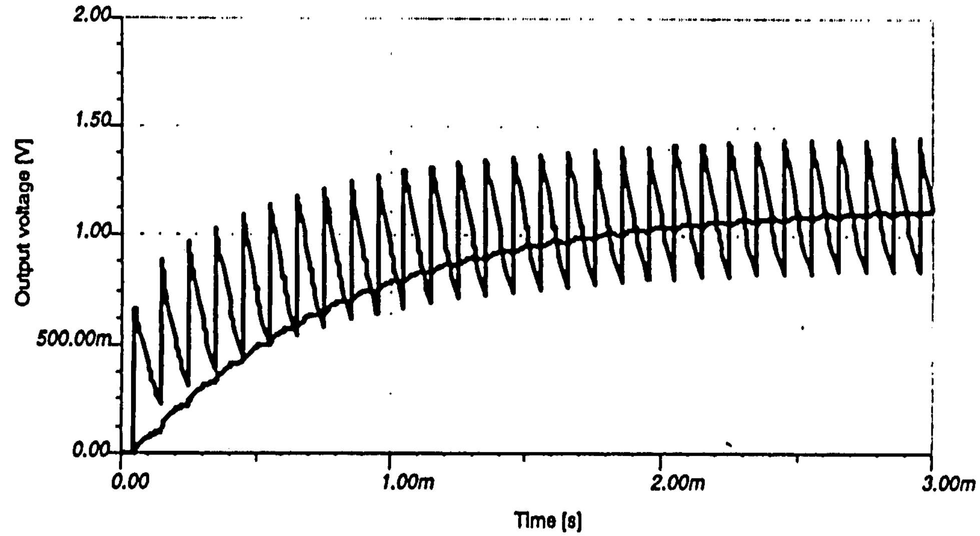
ADAJC431

Input 10kHz



T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator



(b) op2 and op3 overlaid

Fig 3:- (a) Basic AAJC with 10kHz input and (b) Waveforms

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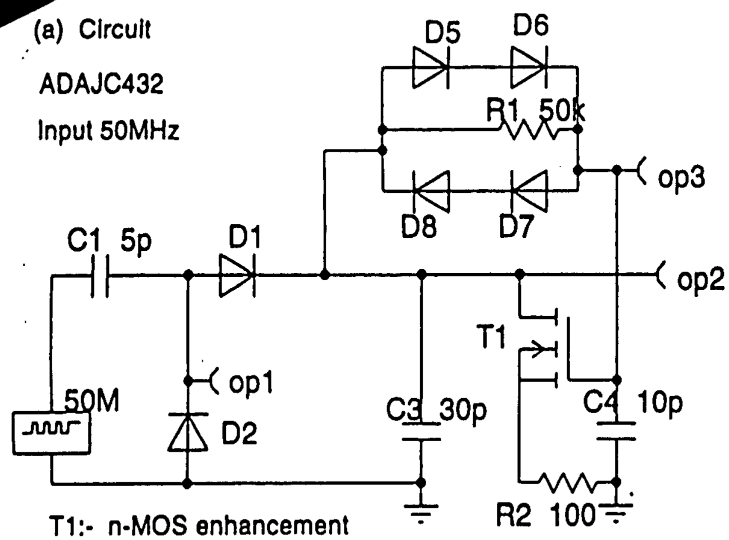
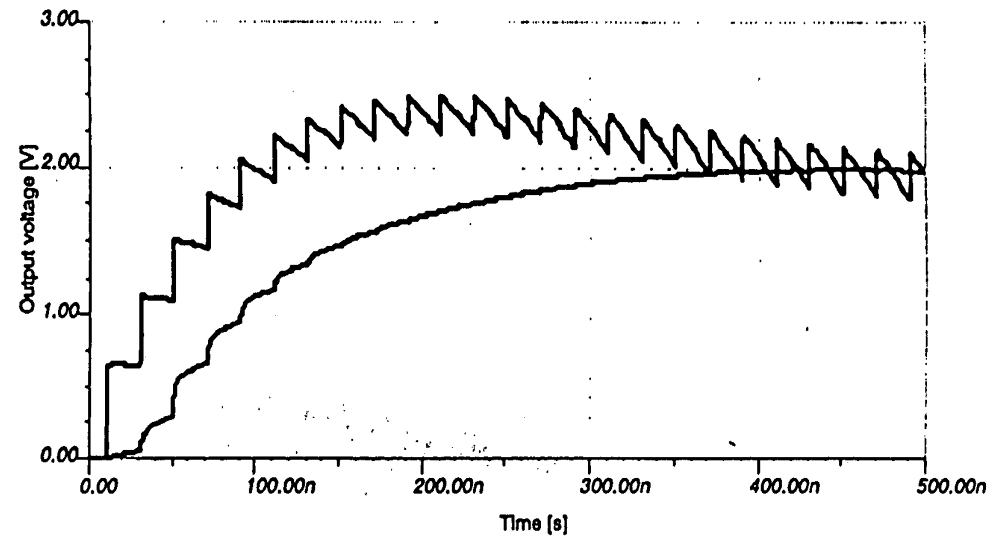


T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator



(b) op2 and op3 overlaid

Fig 4:- (a) Basic AAJC with 50MHz input and (b) Waveforms

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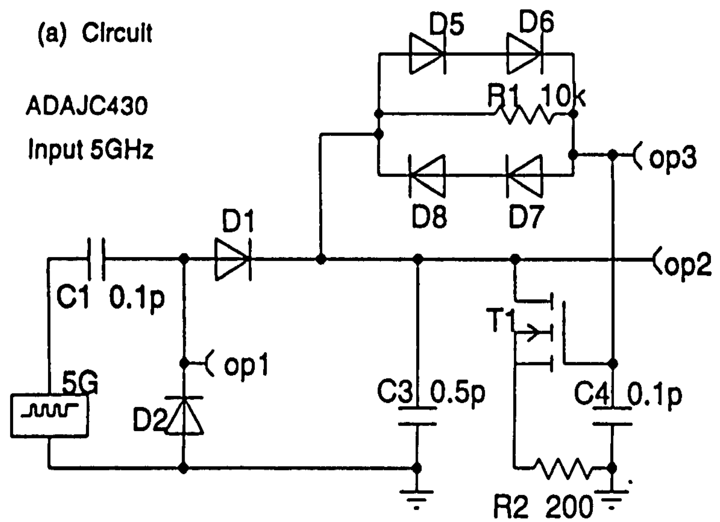
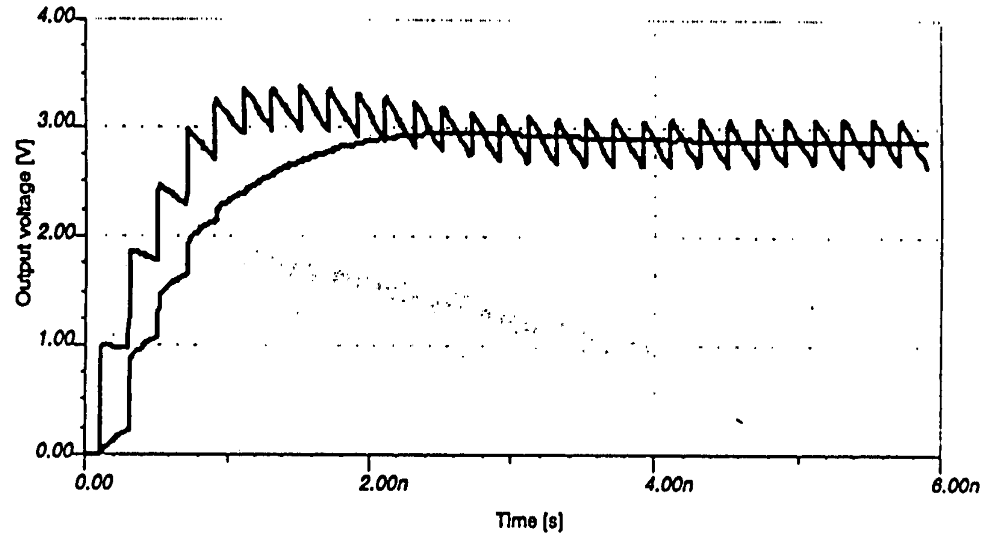
(a) Circuit

ADAJC430
Input 5GHz



T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator



(b) op2 and op3 overlaid

Fig 5:- (a) Basic AAJC with 5GHz input and (b) Waveforms

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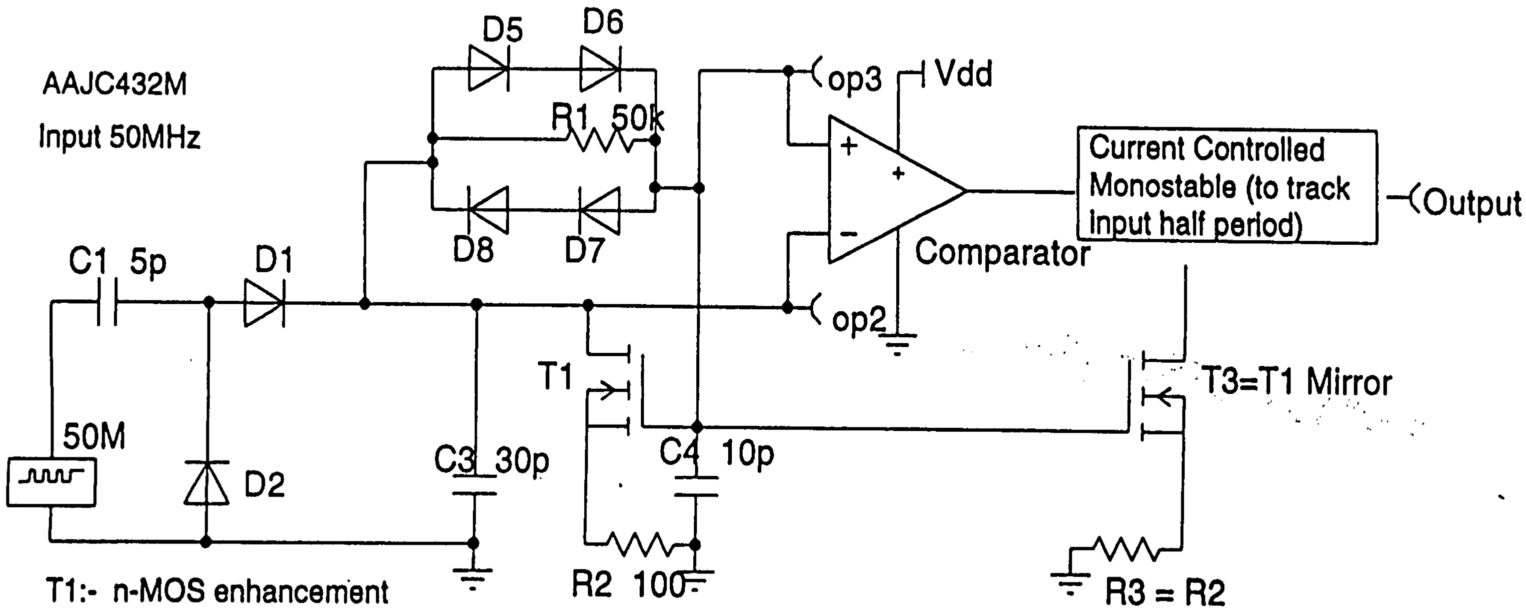
AAJC432M

Input 50MHz



T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Fig 6 AAJC with Comparator and input-tracking Output Monostable

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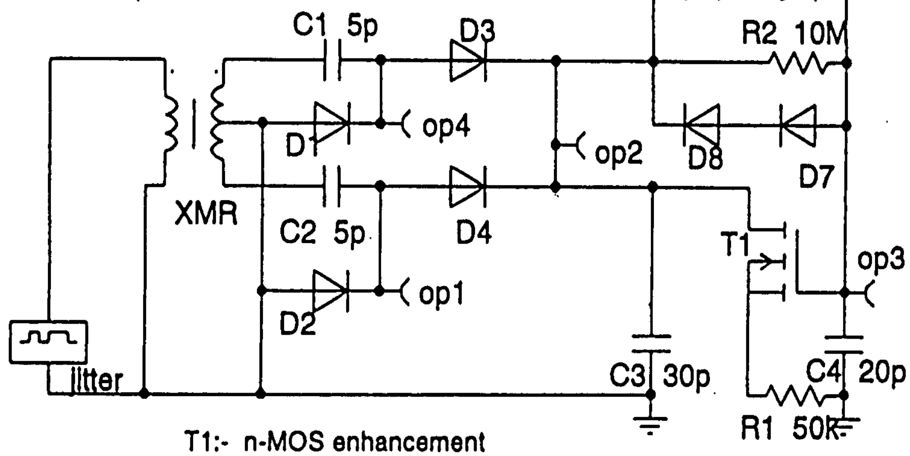
(a) Circuit

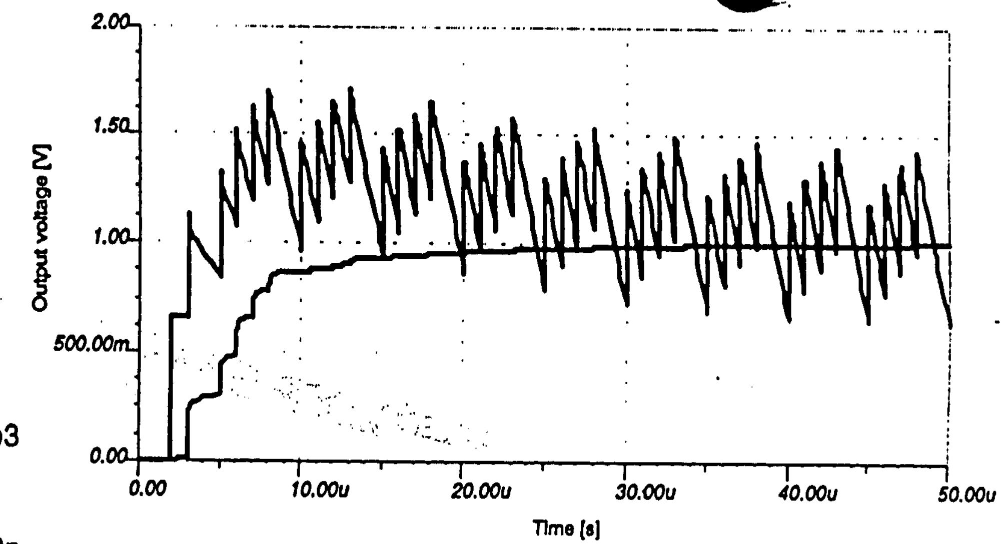
ADAJC45
Jitter Input



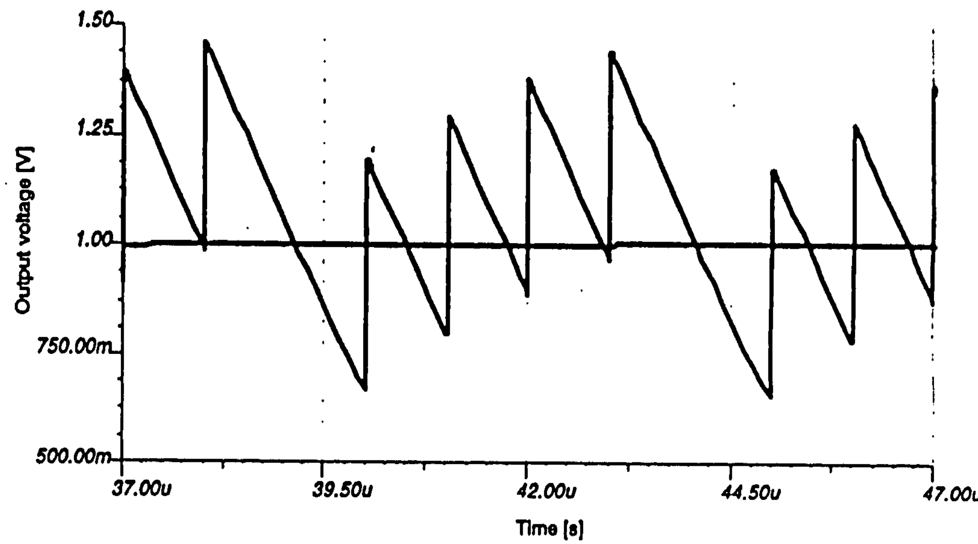
T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of ~~300~~ 150 degrees
=Time Jitter of 1usec in 2.4usec at 1/3 rate



(b) op2 and op3 overlaid



(c) op2 and op3 overlaid and expanded

Fig7:- (a) Basic Frequency Doubling AAJC with jitter input and Waveforms (b) and (c)

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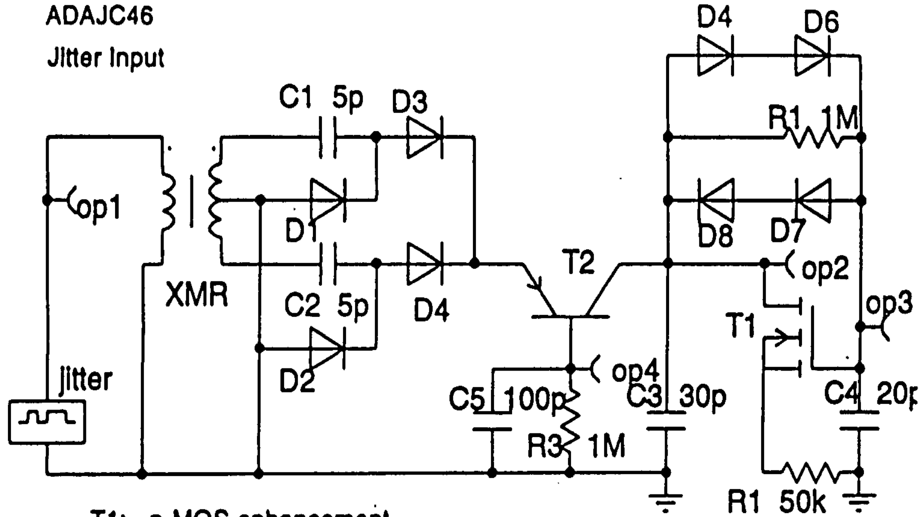
(a) Circuit

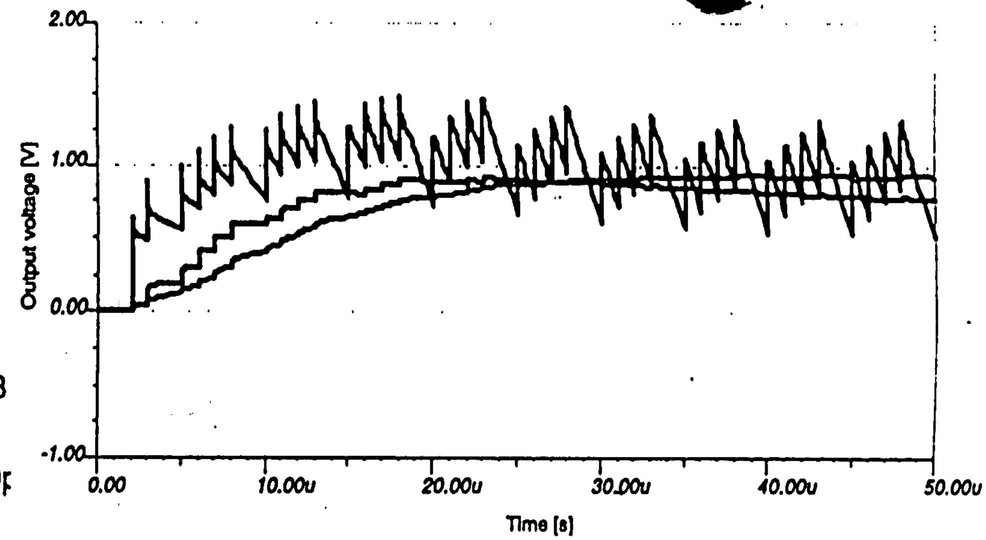
ADAJC46
Jitter Input



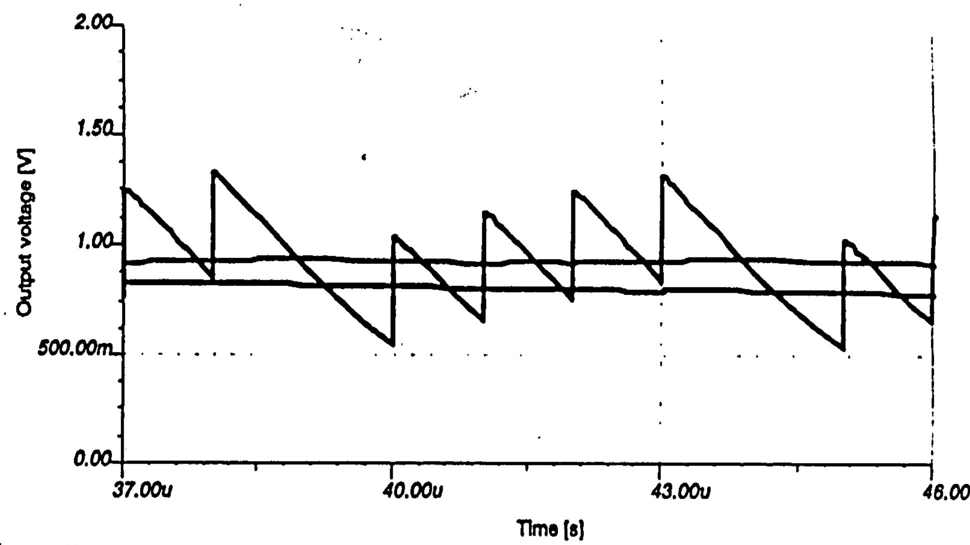
T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 150 degrees
=Time Jitter of 1usec in 2.4usec at 1/3 rate



(b) op2, op3 and op4 overlaid

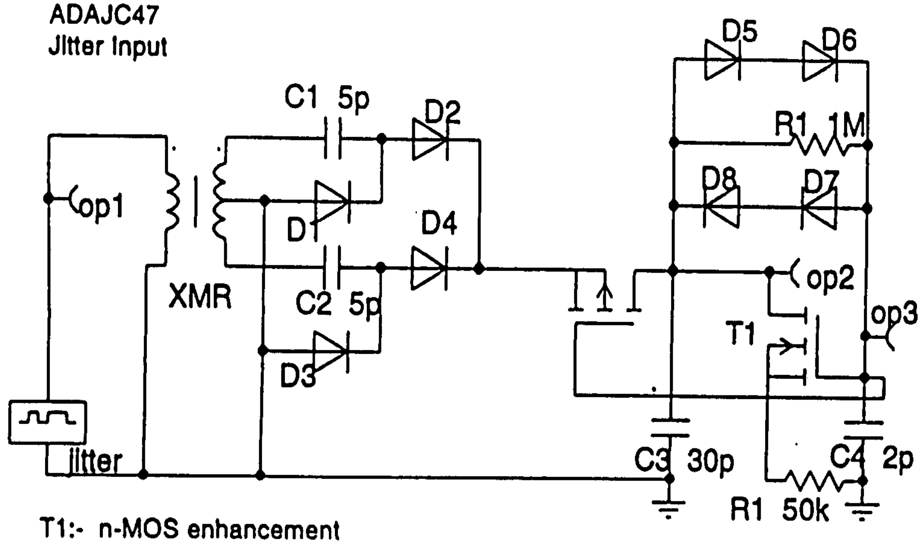


(c) op2, op3 and op4 overlaid and expanded

Fig 8:- (a) Frequency Doubling AAJC with grounded base charge pump and jitter input, and Waveforms (b) and (c)

(a) Circuit

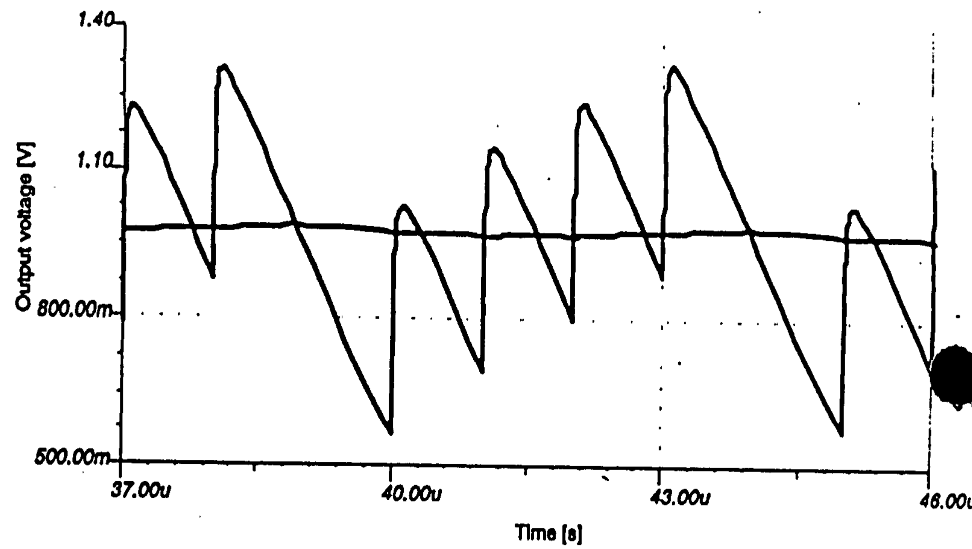
ADAJC47
Jitter Input



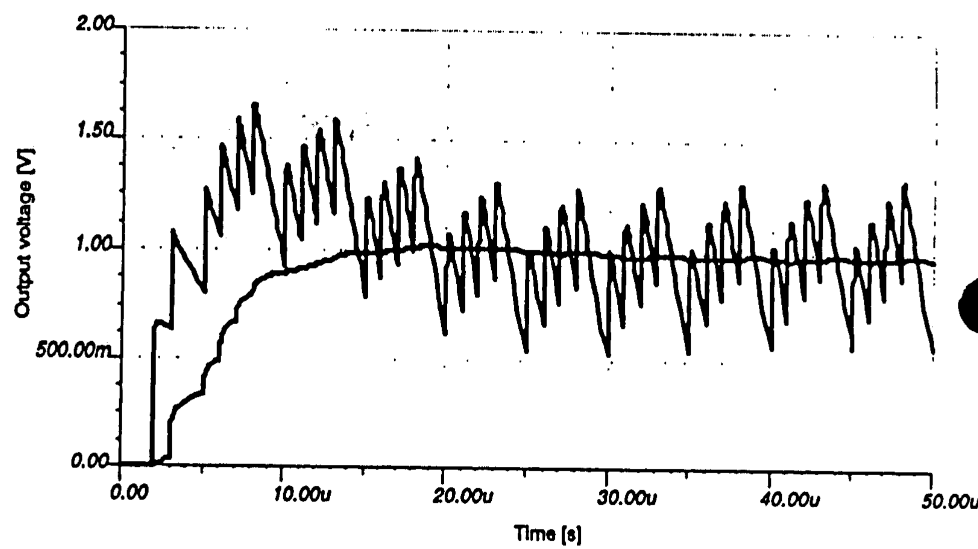
T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 300 degrees
=Time Jitter of 1usec in 2.4usec at 1/3 rate



(b) op2 and op3 overlaid



(c) op2 and op3 overlaid and expanded

Fig 9:- (a) Frequency Doubling AAJC with grounded gate charge pump and jitter input, and Waveforms (b) and (c)

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